SR040

Ultra-Wideband Transceiver

Rev. 1.2 — 29 September 2021 Product short data sheet
666312 COMPANY PUBLIC

1 General description

The SR040 is a fully integrated single chip Impulse Radio Ultra-Wideband (IR-UWB) low-energy transceiver IC compliant to IEEE 802.15.4/4z HRP UWB PHY (see [1] and [2]) and supports FiRa consortium MAC and PHY. It is designed for Ranging applications in an IOT environment. It can be used for 2-way ranging achieving an accuracy of ±10cm in non-line of sight; and one way ranging for Time Difference of Arrival.

2 Features and benefits

SR040 supports the following features.

- IEEE 802.15.4z HRP PHY compliant (see [1] and [2])
- Supports SHF UWB bands from 6.0 GHz to 8.5 GHz for worldwide use
- Programmable transmitter output power of up to 10.5 dBm peak
- Support of 128 MHz PRF (HPRF) mode, doubles available mean TX power compared to IEEE 802.15.4 (see [1])
- Supply voltage 1.8 V to 3.6 V
- Configurable current limiter for applications with coin cell battery supply
- Supports 2-way ranging and TDoA
- Scrambled Timestamp Sequence (STS) generation compliant to NIST SP 800-90A (see [5])
- 6 mm x 6 mm 40-pin QFN package with 0.5 mm lead pitch and wettable flanks
- Based on ARM® Cortex-M33 with ARM® TrustZone (see [3] and [4])
- FiRa ready MAC and PHY
- Built-in on-chip UWB FW (can be updated in the field)
- No custom programming required on processor
- SPI interface to host CPU

3 Applications

SR040 is targeted for following applications.

- IoT applications with coin cell battery operation
- UWB trackers
- UWB tags

4 Pinning information

4.1 Pinning

SR040 is packaged in an HVQFN40.

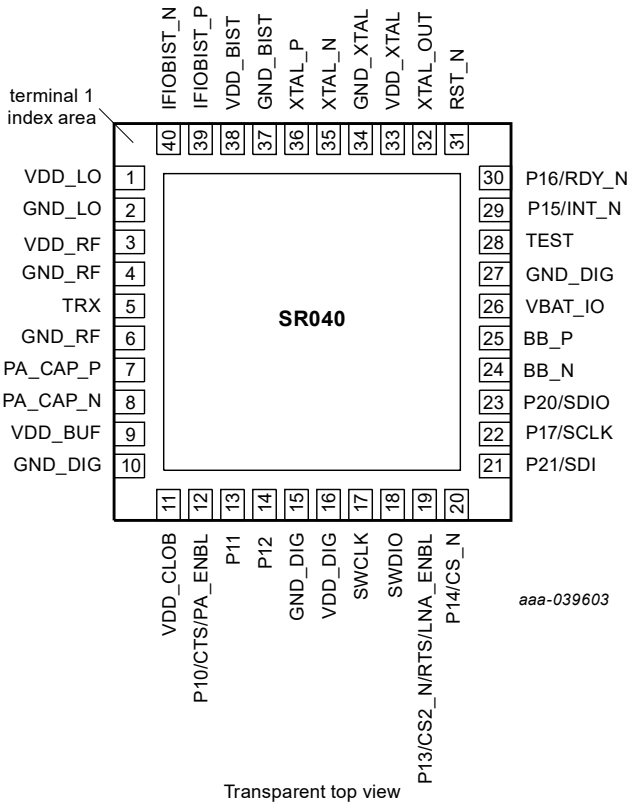

Figure 1. Pinout HVQFN40

4.2 Pin description

Table 1. SR040 pin description

Symbol	Pin	Description
VDD_LO	1	Power supply for local oscillator generation of the analog receiver and transmitter
GND_LO	2	Ground
VDD_RF	3	Power supply for analog receiver and transmitter
GND_RF	4	Ground
TRX	5	Single-ended, RF receiver input and RF transmitter output
GND_RF	6	Ground
PA_CAP_P	7	External decoupling capacitor
PA_CAP_N	8	External decoupling capacitor
VDD_BUF	9	Internally connected to VBAT_IO, supply for global LDO and PA

Table 1. SR040 pin description*...continued*

Symbol	Pin	Description
GND_DIG	10	Ground (digital)
VDD_GLOB	11	Output voltage of the global LDO
P10 / CTS / PA_ENBL [1]	12	Optional external wake source
P11[1]	13	N/A
P12[1]	14	N/A
GND_DIG	15	Ground (digital)
VDD_DIG	16	Power supply for digital domain
SWCLK	17	Debug interface. N/A
SWDIO	18	Debug interface. N/A
P13 [1]	19	Test point
P14 / CS_N [1]	20	GPIO CS_N - Chip Select (active low); input in SPI Slave operation
P21 / SDI [1]	21	GPIO SDI - Data input for SPI full duplex operation
P17 / SCLK [1]	22	GPIO SCLK - Data clock for SPI operation; input in SPI Slave operation
P20 / SDIO [1]	23	GPIO SDIO - Data I/O for SPI operation; output in full duplex operation; input/ output in half-duplex operation
BB_N	24	External decoupling capacitor
BB_P	25	External decoupling capacitor
VBAT_IO	26	Power supply for digital I/Os and power supply for the chip via current limiter
GND_DIG	27	Ground (digital)
TEST	28	Test pin (must be connected to ground in the application)
P15 / INT_N [1]	29	GPIO INT_N - Interrupt output (active low) in 6-wire SPI operation
P16 / RDY_N [1]	30	GPIO RDY_N - Ready output (active low) in 6-wire SPI operation
RST_N	31	Reset input (active low), internal pull-up resistor
XTAL_OUT	32	N/A
VDD_XTAL	33	Power supply for XTAL
GND_XTAL	34	Ground
XTAL_N	35	External crystal
XTAL_P	36	External crystal
GND_BIST	37	Ground
VDD_BIST	38	Power supply for BIST, ADC, DAC, system clock generation
IFIOBIST_P	39	N/A, Ground
IFIOBIST_N	40	N/A, Ground

[1] Unused GPIO pins should be left open.

5 Functional description

This chapter provides high-level information on SR040 architecture and subsystems along with functional usage. The SR040 can be connected to a host controller through physical interface of SPI. The SR040 supports operation in 3 V power supply. SR040 has one RX and one TX.

5.1 CPU subsystem

SR040 is based on ARM® Cortex®-M33 processor (see [3]) and implements the ARM® TrustZone extension (see [4]). FiRa MAC and PHY FW is implemented on ARM® Cortex®-M33. UWB chip provides SPI interface toward host processor, which allows driving different UWB features from connected host.

5.1.1 Serial peripheral interface (SPI)

A single serial peripheral interface (SPI) block is provided. It supports the following key features.

- SPI data rate up to 10 MHz supported
- SPI slave operation supported
- Data transmissions of 1 to 16 bit supported directly. Larger frames supported by software
- The SPI building block supports separate transmit and receive FIFO buffers with 8 entries each with 16-bit width
- The device supports wake-up from power-saving modes through events on the SPI interface

Table 2. SPI Pin description

Pin	Type	Function	Description
P17 / SCLK	I/O	SCK	Serial Clock for SPI. SCK is a clock signal used to synchronize the transfer of data. It is driven by the master and received by the slave. When the SPI interface is used, the clock is programmable to be active high or active-low. SCK only switches during a data transfer. It is driven whenever the Master bit in CFG equals 1, regardless of the state of the Enable bit.
P21 / SDI	Input	MOSI	Data input when SPI is a slave in 4-wire operation, it clocks in serial data from this signal.
P20 / SDIO	I/O	MISO	Data output when SPI is a slave in 4-wire operation.
P14 / CS_N	I/O	SSEL0	Slave Select 0 for SPI. By default, this signal is active low but can be selected to operate as active high. When the SPI is a slave, any SSEL in an active state indicates that this slave is being addressed. The SSEL pin is driven. .
P13 / CS2_N	I/O	SSEL1	Not supported
		SSEL2	Not supported
		SSEL3	Not supported

In addition to the 4-wire mode, two additional and optional control lines are provided (resulting in the 6-wire mode). These are the RDY_N (Ready not) and the INT_N (Interrupt not).

The RDY_N signal handshakes the CS_N (generated from the host) in order to ensure that the SPI transfer will be successful. CS_N can be understood as a request to send (RTS) and the RDY_N as clear to send (CTS). Using the RDY_N signal is optional, and the host can always rely on waiting some predefined time to transmit a command or read a response. The RDY_N signal is activated (active low) always after CS_N activation and deactivated after CS_N deactivation. When the host (SPI master) accidentally transmits a command while the RDY_N is not activated, the SR040 will ignore the transfer.

The purpose of the INT_N signal is to inform the host that there are data to be read from the device, or an event has occurred which needs to be inspected by the host. Using the INT_N signal is optional, and the host can always rely on polling the SR040 for its status and act accordingly. The INT_N signal is active low. It can be activated at any time, because events that trigger the INT_N are asynchronous and cannot be foreseen. The INT_N is active as long as a pending event isn't read out. INT_N is cleared after the SPI transmission was started by the host activating CS_N and the SR040 handshaking this by activating RDY_N. If another event is pending, INT_N is reactivated.

SPI interfaces typically allow configuration of clock phase and polarity. These are referred as numbered SPI modes, as described in Table 3 and Figure 2. CPOL and CPHA are configured by internal CFG register. CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity.

Table 3. SPI mode summary

CPOL	CPHA	SPI Mode	Description	SCK Rest state	SCK data change edge	SCK data sample edge
0	0	0	The SPI captures serial data on the first clock transition of the transfer (when the clock changes away from the rest state). Data is changed on the following edge.	Low	Falling	Rising
0	1	1	The SPI changes serial data on the first clock transition of the transfer (when the clock changes away from the rest state). Data is captured on the following edge.	Low	Rising	Falling
1	0	2	Same as mode 0 with SCK inverted.	High	Rising	Falling
1	1	3	Same as mode 0 with SCK inverted.	High	Falling	Rising

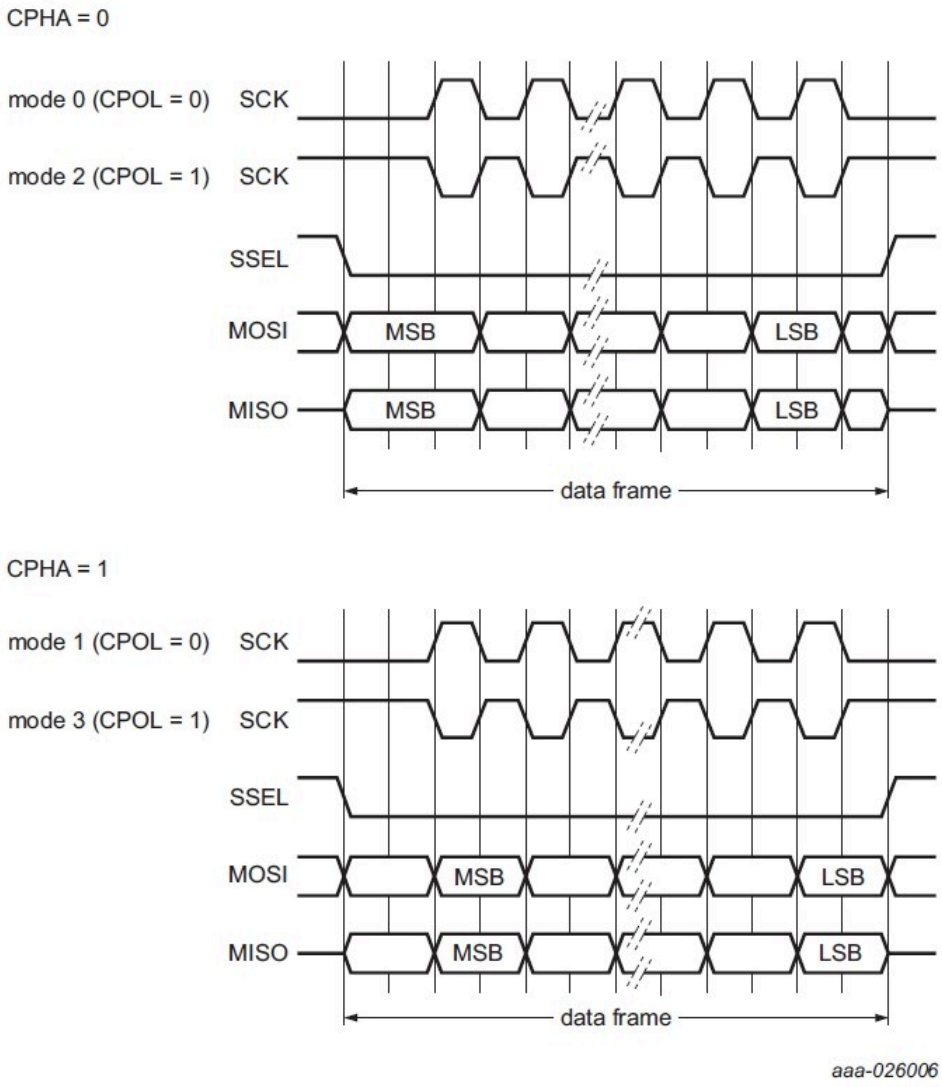

Figure 2. SR040 SPI data frame

5.2 Power management

5.2.1 Modes of operation

The device supports operation in a 3 V environment supporting the following supply use cases:

- Device and digital interface supplied with regulated 3 V (3.3 V) supply
  - Digital signaling between all devices in the system is done at 3 V (3.3 V) level.
- Device and digital interface supplied with a 3 V battery
  - Digital signaling between all devices in the system is done at battery voltage level. MCU and SR040 use same Vbat, then no level translators are required.
  - An energy storage capacitor is required to deliver the required peak current during frame reception and frame transmission.

5.2.2 Power modes state diagram

Figure 3 shows different power states and transition of those power states.

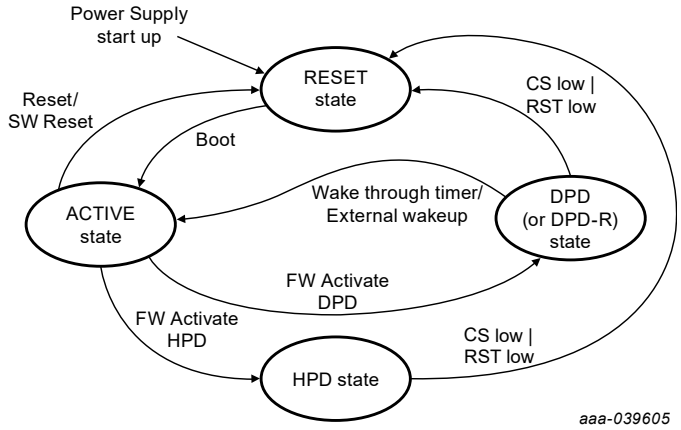

Figure 3. SR040 power modes state diagram

5.2.3 Current limiter

The current limiter is intended for applications with coin cell battery supply, to maximize the lifetime of the battery. It minimizes battery stress by limiting the maximal current drawn by the IC. The current limit is configurable by SW.

6 Recommended operating conditions

Table 4. Operating conditions

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	Operating frequency Ch5, Ch6, Ch8 and Ch9	6.24	-	8.24	GHz
Operating Temperature	All specification parameters fulfilled	-30	+25	+85	°C
Supply voltage range[1]	Device fully functional	1.8	-	3.6	V

[1] TX PA peak power shall not be set higher than 9dBm between 1.8V and 2.4V

7 Glossary

Table 5. Glossary

ADC	Analog to Digital Converter
BIST	Built-in Self-Test
DAC	Digital to Analog Converter
DPD	Deep Power Down
HPD	Hard Power Down
PER	Packet Error Rate
RF	Radio Frequency
RX	Receiver
SHF	Super High Frequency
SPI	Serial Peripheral Interface
STS	Scrambled Timestamp Sequence
SWD	Serial Wire Debug
TDoA	Time Difference of Arrival
ToF	Time of Flight
TX	Transmitter
TRX	Transmitter Receiver
UWB	Ultra Wideband

8 References

[1] IEEE Std 802.15.4™-2015 (Revision of IEEE Std 802.15.4-2011) IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. https://standards.ieee.org/

[2] **IEEE Std 802.15.4z™-D08** (Draft Revision of IEEE Std 802.15.4-2015) Amendment: Enhanced Ultra Wide-4 Band (UWB) Physical Layers (PHYs) and Associated Ranging Techniques https://www.techstreet.com/ieee/standards/ieee-p802-15-4z?gateway_code=ieee&vendor_id=7291&product_id=2087572

[3] ARM® Cortex®-M33 Processor - Technical Reference Manual Rev. r0p2

[4] ARM® TrustZone

[5] NIST Special Publication 800-90A Revision 1 2015. Recommendation for Random Number Generation Using Deterministic Random Bit Generators

9 Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
666312	2021-09-29	Product short data sheet	-	666311
Modifications:	• Update Section 7			
666311	2021-06-11	Product short data sheet	-	666310
Modifications:	• Update in Section 1 • Updates Section 2 • Updates in Table 1 • Updates in Section 5.1 • Deleted Sections "5.2.2 Power supply states" and "5.2.2.1 State Diagram and Power modes" • Added Section 5.2.2 • Glossary updated			
666310	2021-03-22	Product short data sheet	-	-
Modifications:	• Initial version			

10 Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Tables

Figures

Contents

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